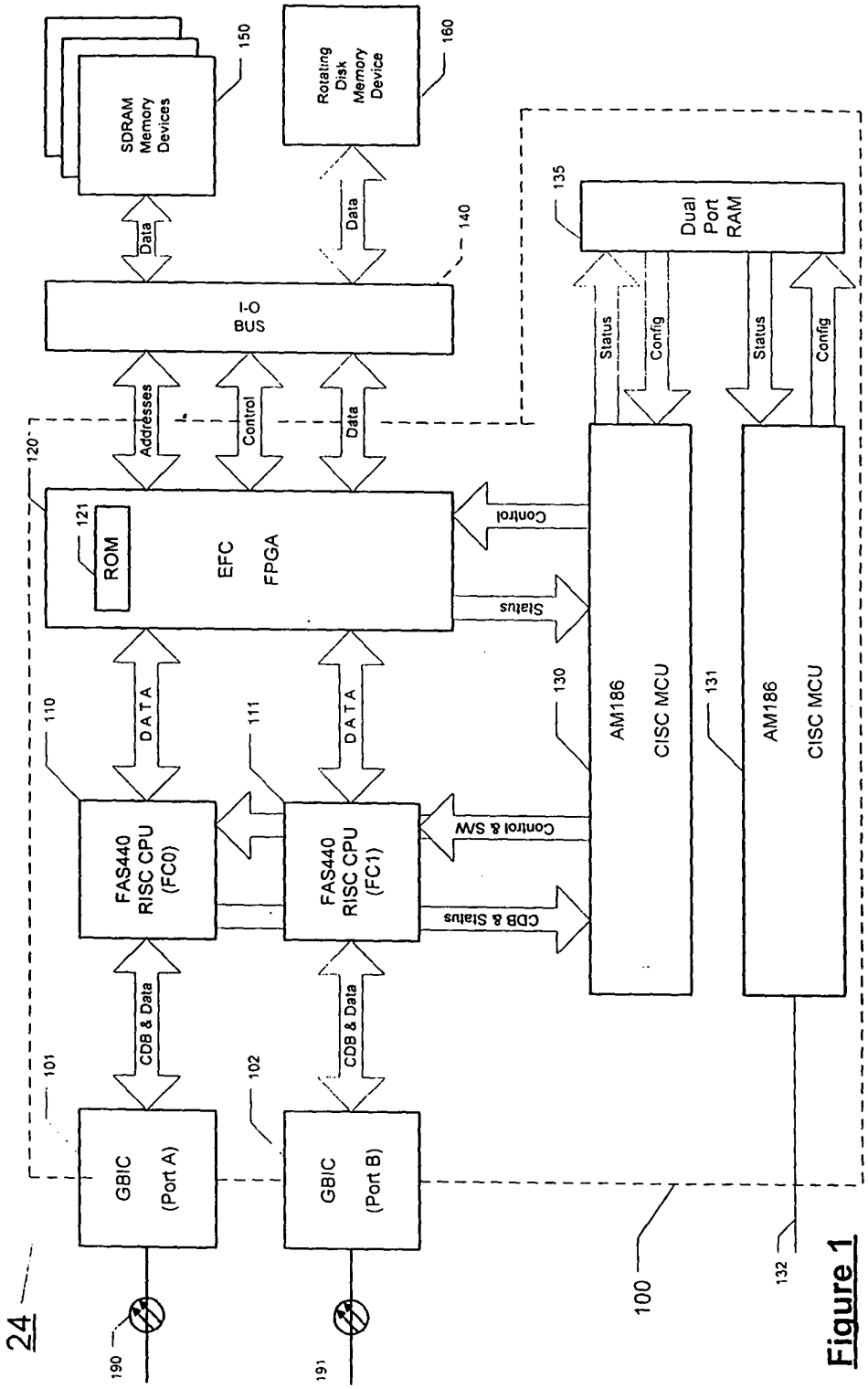

24
SDRAM Memory Devices
150
Rotating Disk Memory Device
160
Data
Data
140
I-O BUS
Addresses
Control
Data
120
121
ROM
EFC FPGA
Control
Status
110
111
DATA
DATA
FAS440 RISC CPU (FC0)
FAS440 RISC CPU (FC1)
CDB & Data
CDB & Data
101
102
GBIC (Port A)
GBIC (Port B)
190
191
135
Dual Port RAM
Status
Config
Status
Config
130
AM186 CISC MCU
131
AM186 CISC MCU
Control & S/W
CDB & Status
100
132

Figure 1

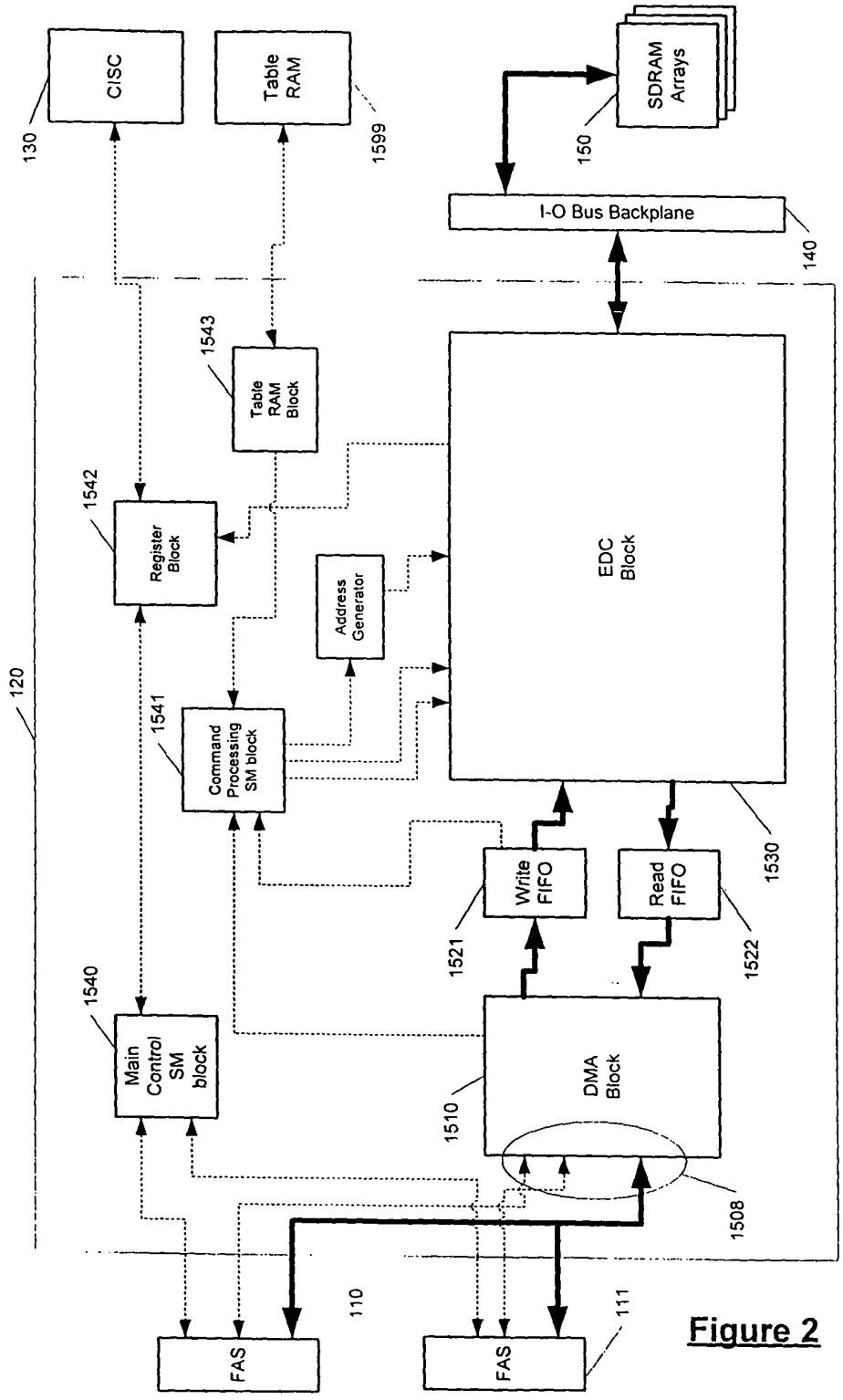
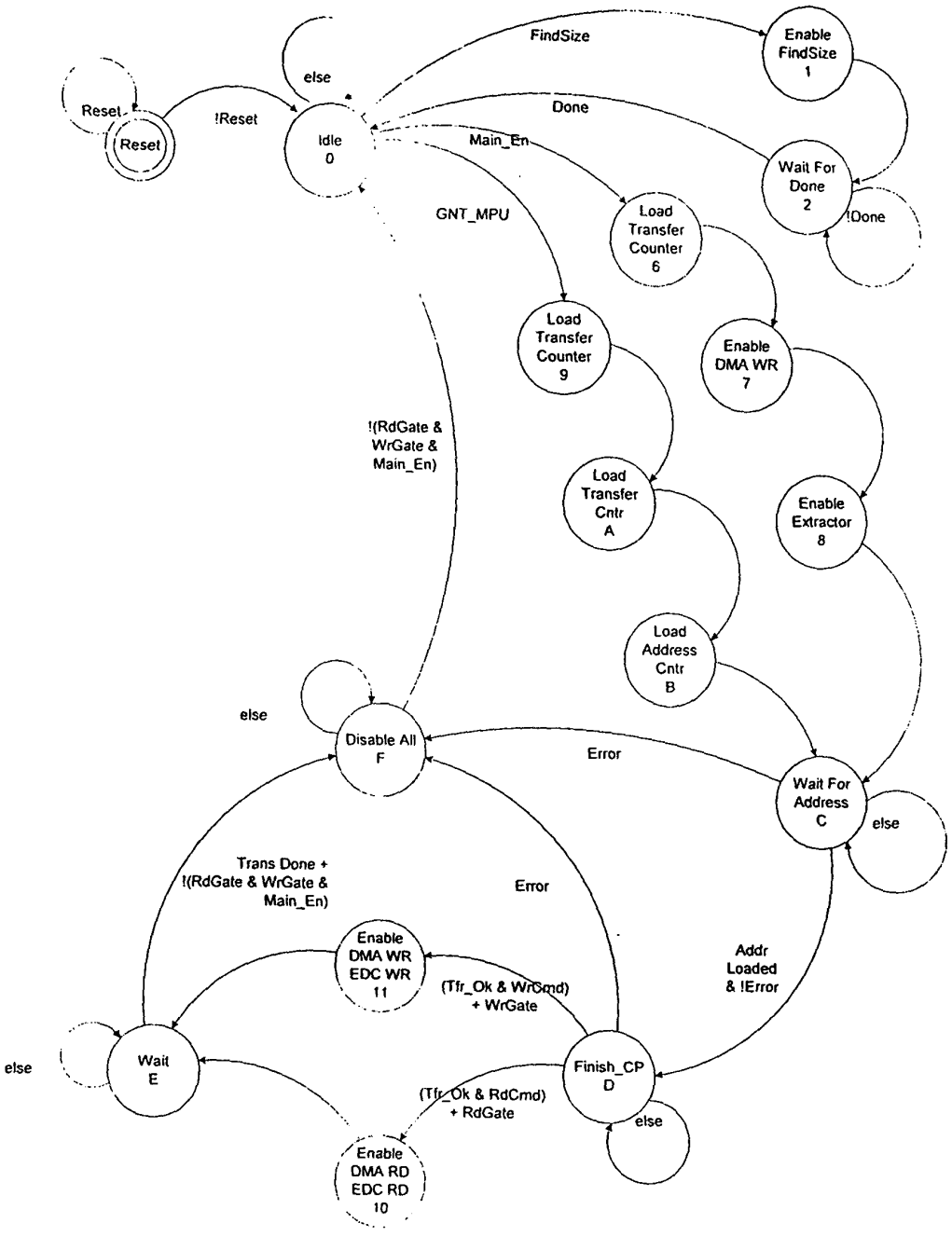
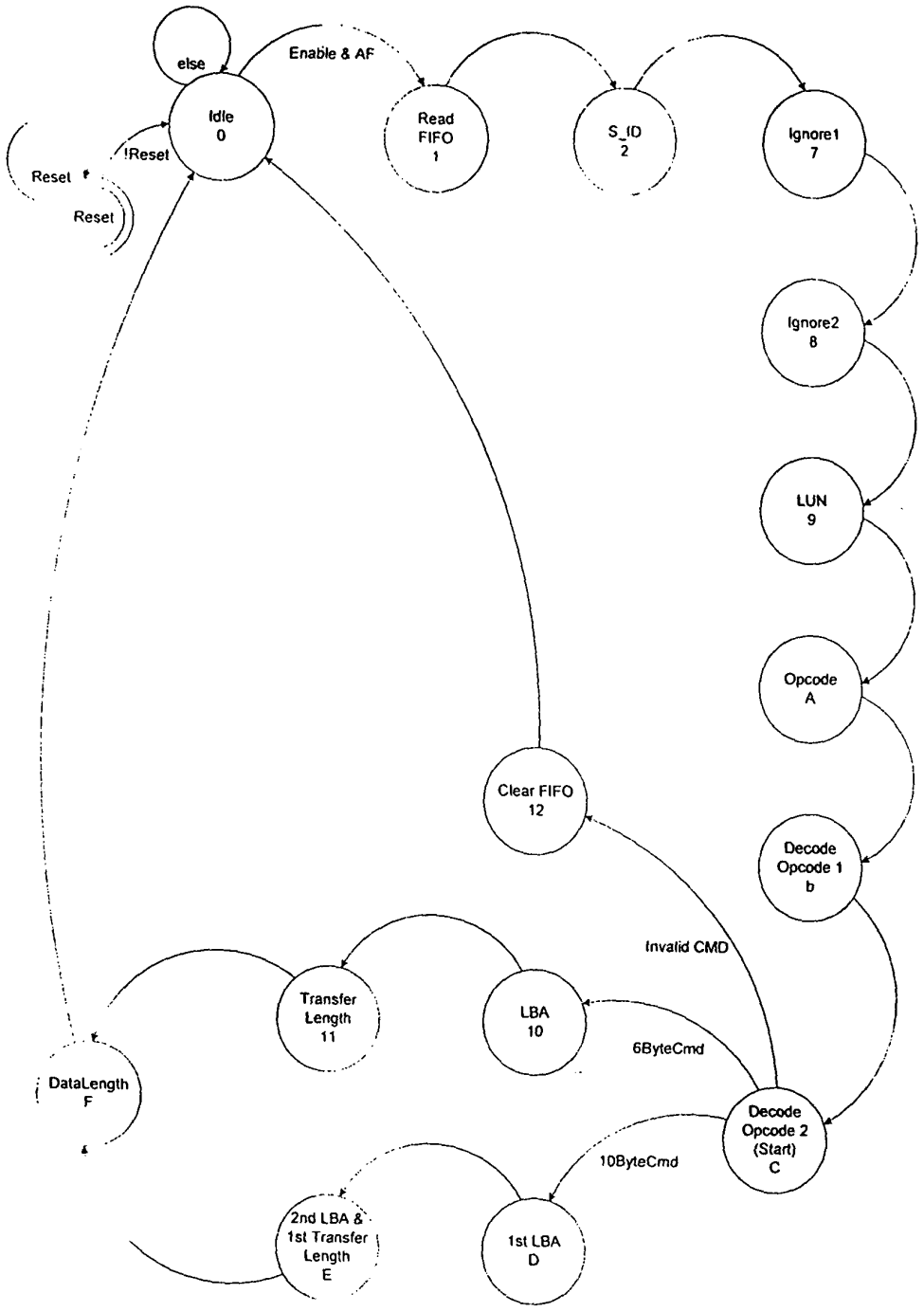

CISC
130
Table RAM
1599
SDRAM Arrays
150
I-O Bus Backplane
140
1543
Table RAM Block
1542
Register Block
Address Generator
EDC Block
120
1541
Command Processing SM block
1530
Write FIFO
Read FIFO
1521
1522
1540
Main Control SM block
DMA Block
1510
1508
110
111
FAS
FAS

Figure 2




Main State Diagram

**Figur 3**




Extractor State Diagram

**Figure 4**

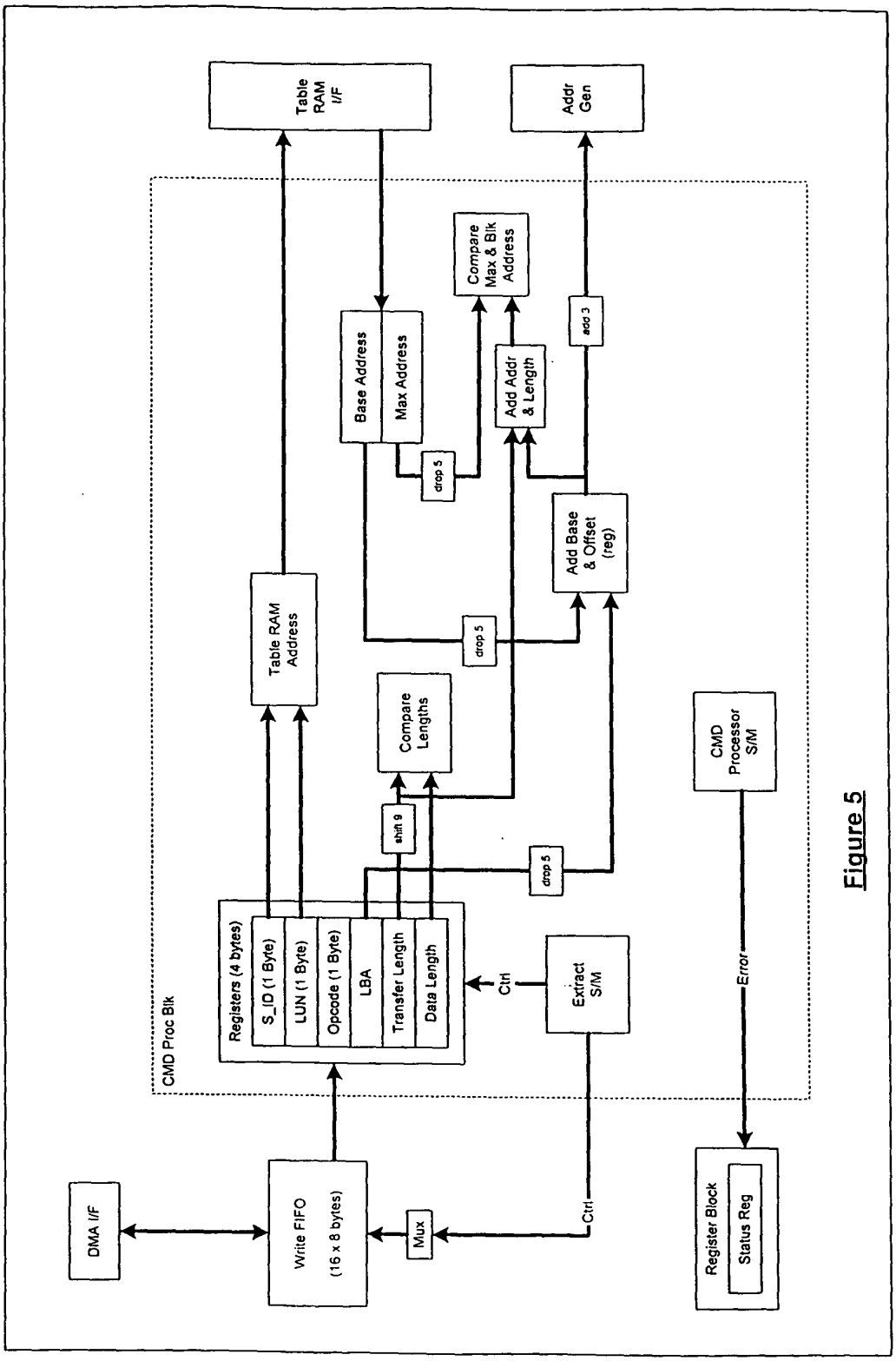


Table RAM I/F
Addr Gen
Compare Max & Blk Address
Base Address
Max Address
add 3
drop 5
Add Addr & Length
Add Base & Offset (reg)
Table RAM Address
drop 5
Compare Lengths
shift 9
drop 5
CMD Processor S/M
CMD Proc Blk
Registers (4 bytes)
S_ID (1 Byte)
LUN (1 Byte)
Opcode (1 Byte)
LBA
Transfer Length
Data Length
Ctrl
Extract S/M
Error
DMA I/F
Write FIFO (16 x 8 bytes)
Mux
Ctrl
Register Block
Status Reg

Figure 5

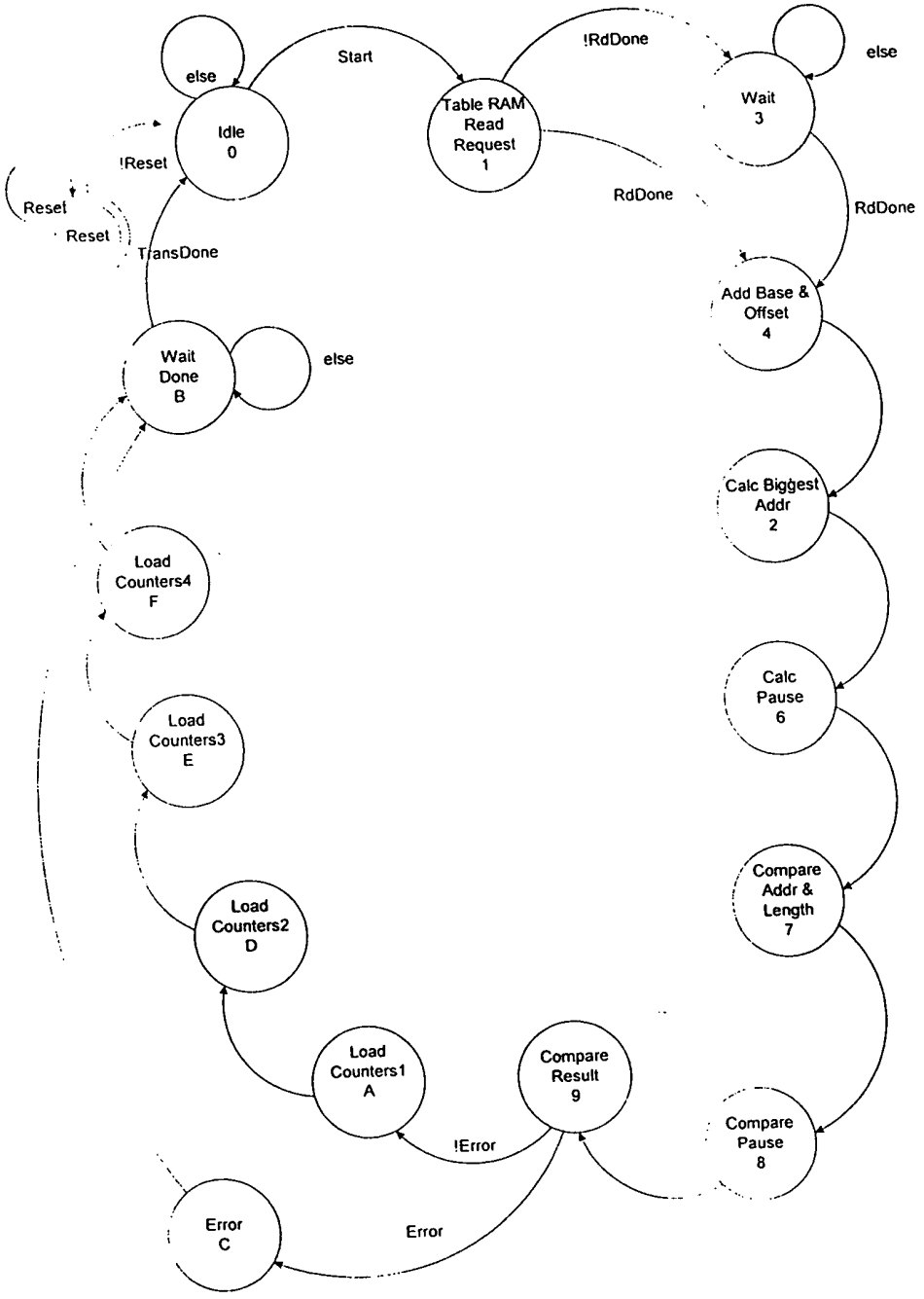



Figure 6

CMD Processor State Diagram

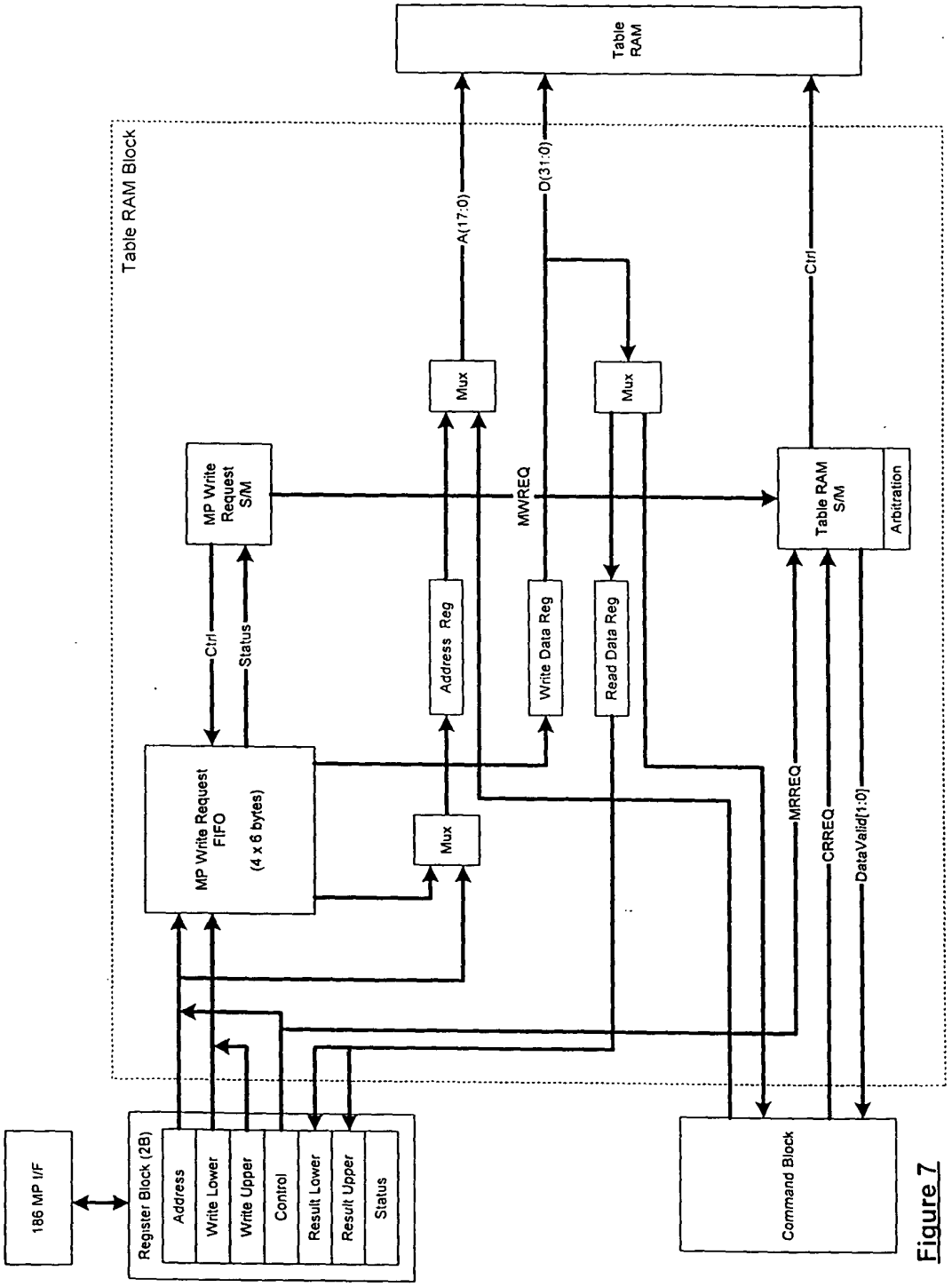
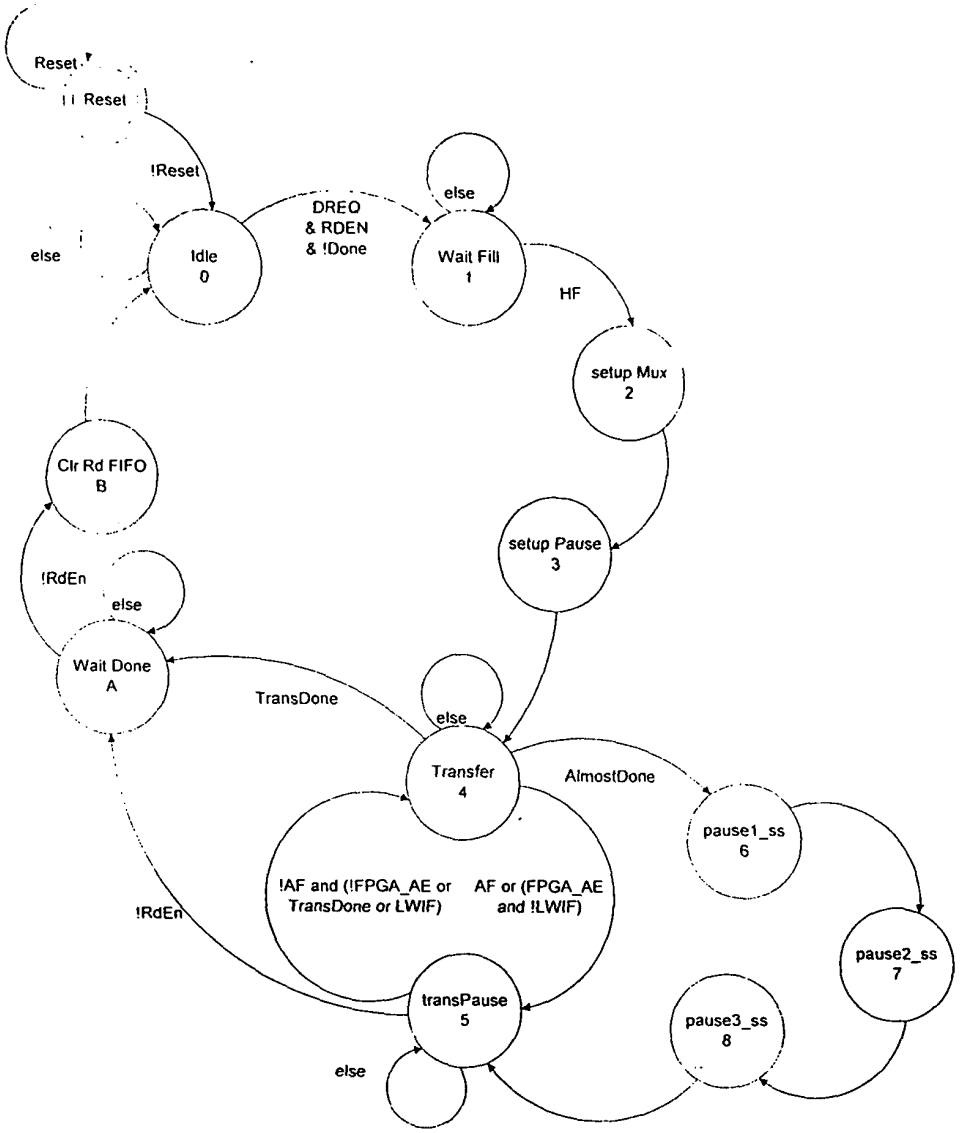


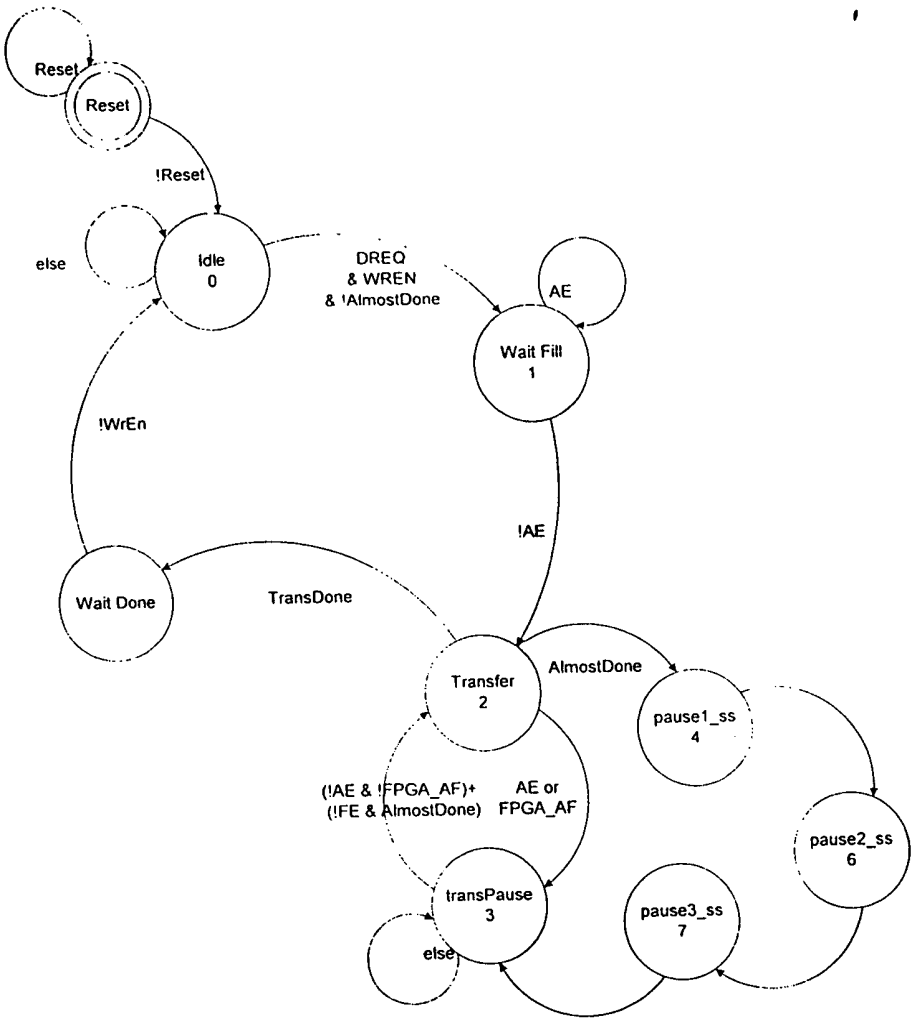
Table RAM
Table RAM Block
A(17:0)
D(31:0)
Ctrl
Mux
Mux
MP Write Request S/M
MWREQ
Table RAM S/M
Arbitration
Address Reg
Write Data Reg
Read Data Reg
Ctrl
Status
MP Write Request FIFO (4 x 6 bytes)
Mux
MRREQ
CRREQ
DataValid[1:0]
186 MP I/F
Register Block (2B)
Address
Write Lower
Write Upper
Control
Result Lower
Result Upper
Status
Command Block

Figure 7




DMA Read State Diagram

**Figure 8**




DMA Write State Diagram

**Figure 9**

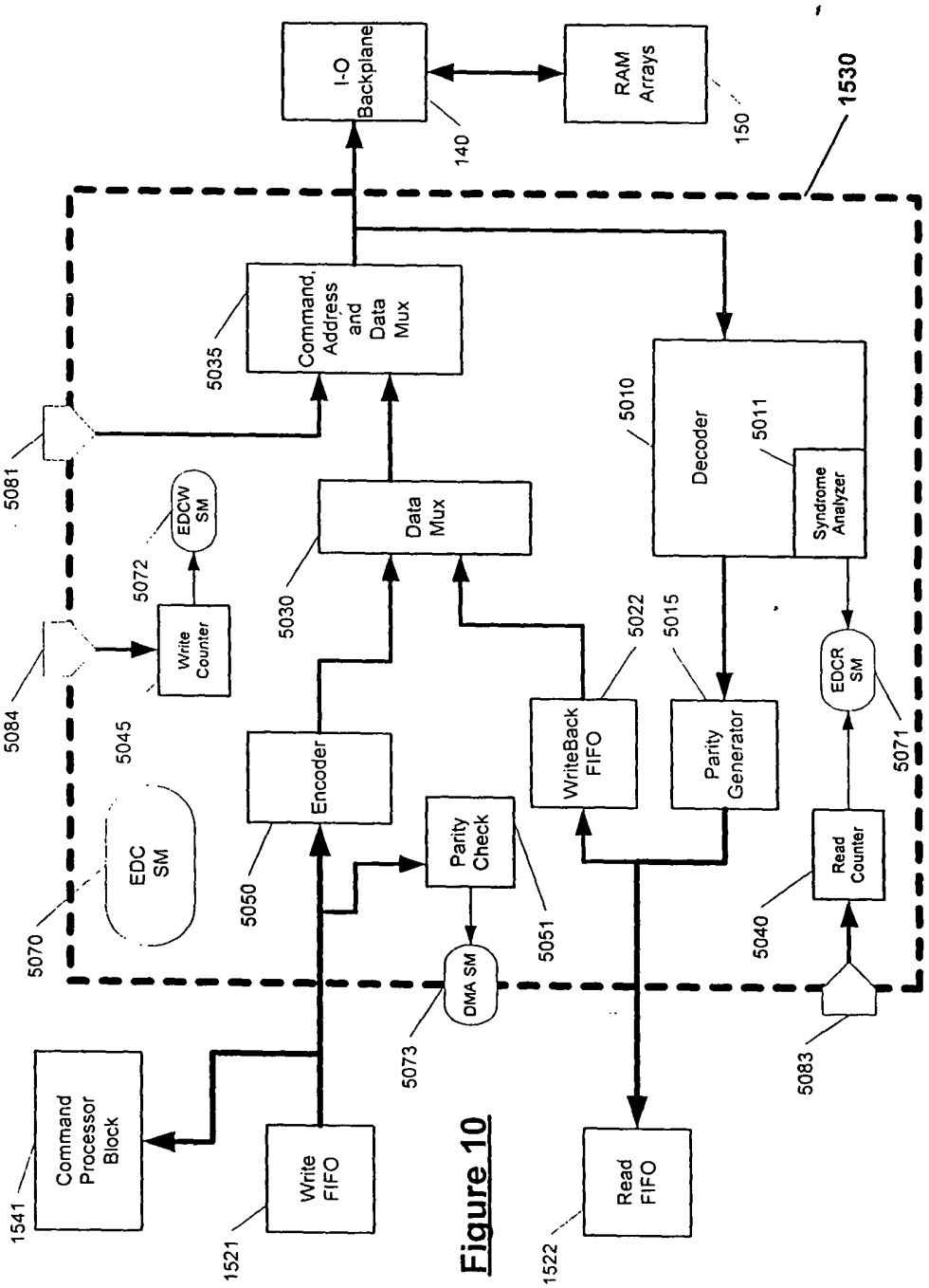
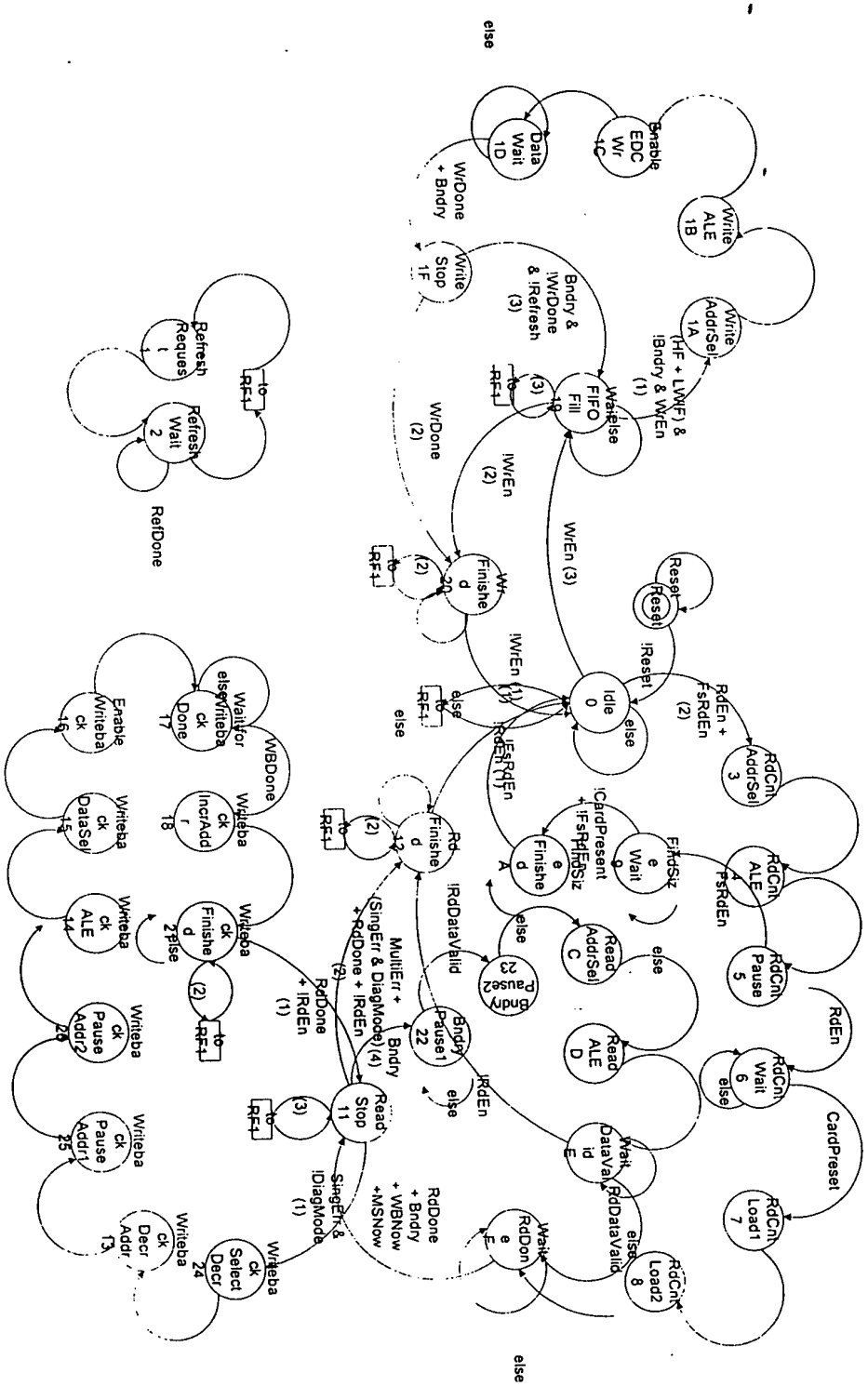
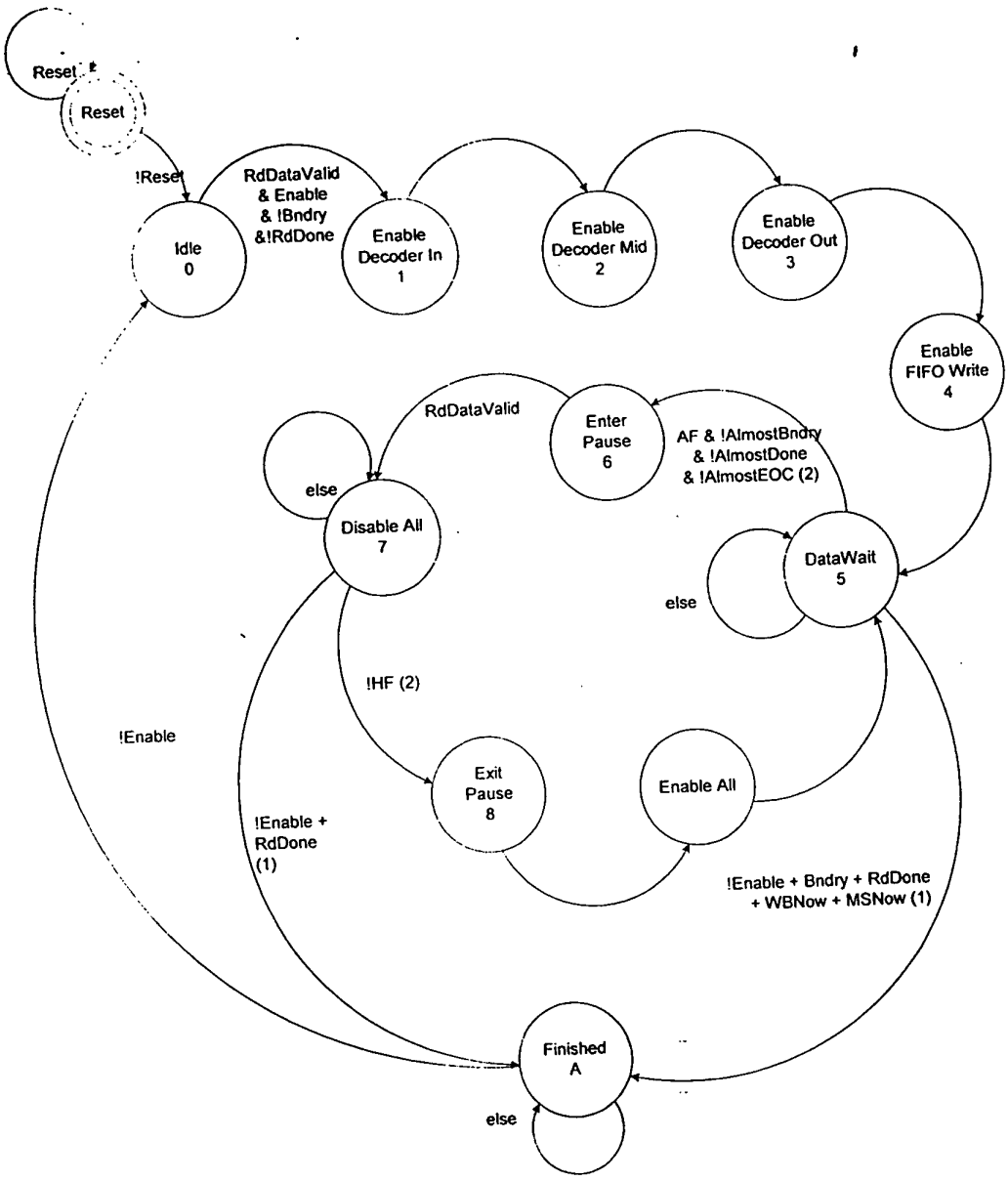

I-O Backplane
140
RAM Arrays
150
1530
Command, Address and Data Mux
5035
Decoder
5010
Syndrome Analyzer
5011
5081
EDCW SM
5072
Write Counter
5084
Data Mux
5030
5022
5015
EDCR SM
5071
5045
EDC SM
5070
Encoder
5050
Parity Check
5051
WriteBack FIFO
Parity Generator
Read Counter
5040
DMA SM
5073
5083
Command Processor Block
1541
Write FIFO
1521
Read FIFO
1522

Figure 10



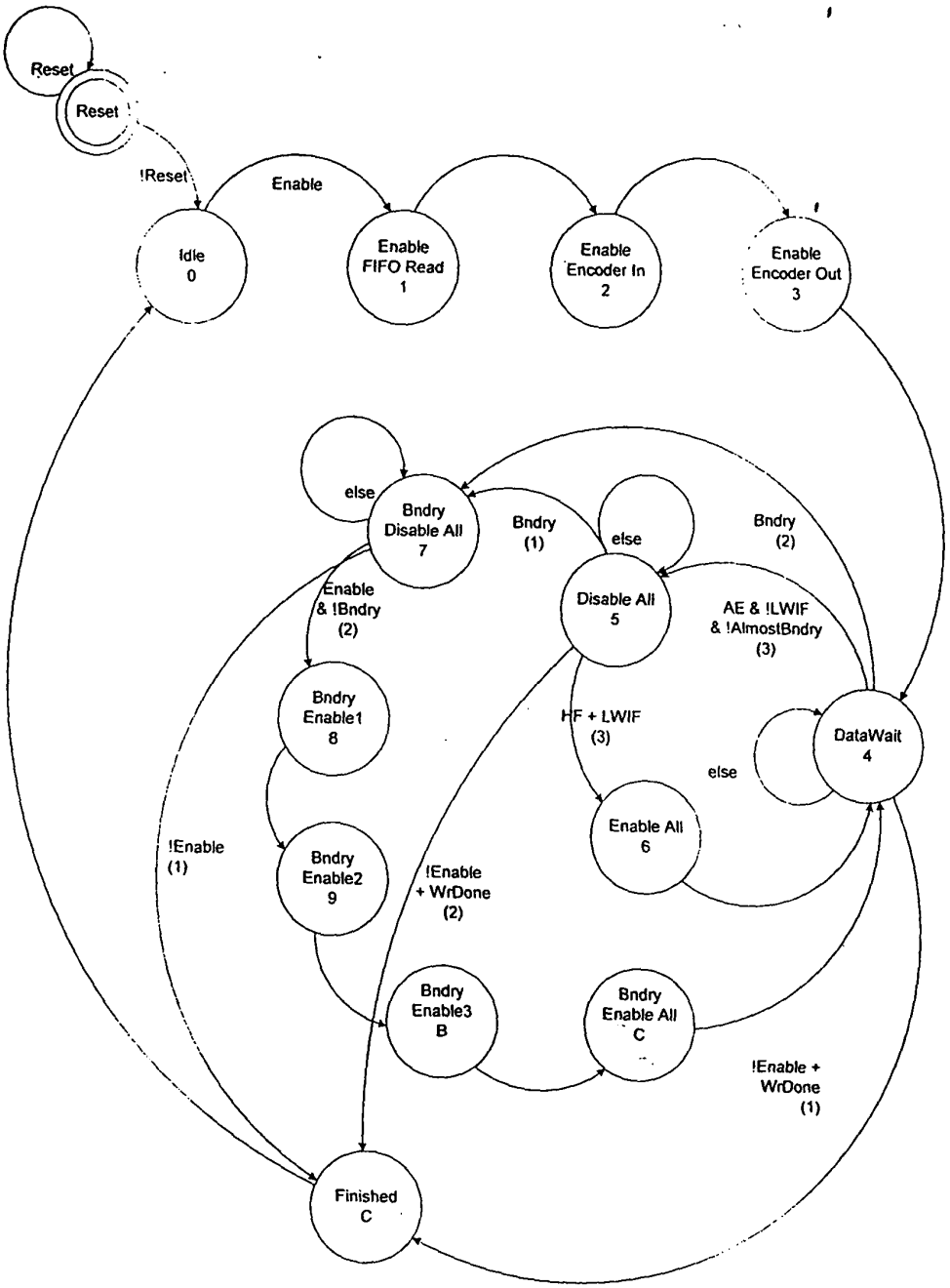

EDC State Diagram

**Figure 11**




EDC Read State Diagram

**Figure 12**




EDC Write State Diagram

**Figure 13**